

U.S. Patent Application Serial No. 10/709,096
Amendment filed September 7, 2006
Reply to OA dated June 29, 2006

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 4 (Canceled).

Claim 5 (Currently Amended): The electronic parts packaging structure according to claim [[3]] 11, wherein the normal via hole is arranged in a position that is away from the connection pad in excess of 200 μ m.

Claim 6 (Currently Amended): A wiring substrate according to claim [[3]] 11, wherein a via post filled in the dummy via hole is formed between an upper surface of the via post and a lower surface of the connection pad or the wiring pattern via the insulating film.

Claim 7 (Currently Amended): A wiring substrate according to claim [[1 or 2]] 11, wherein the wiring substrate has a plurality of connection pads corresponding to a plurality of bumps of the electronic parts, and a plurality of via holes associated with the plurality of connection pads, and a diameter of the via holes formed in portions corresponding to both end portions of the

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electronic parts is set larger than a diameter of the via hole formed in a portion corresponding to a center portion of the electronic parts, in an oscillation direction of an ultrasonic wave applied when the electronic parts is packaged onto the wiring substrate by the ultrasonic flip-chip packaging.

Claim 8 (Currently Amended): The electronic parts packaging structure according to claim [[1 or 2]] 11, wherein the insulating film on the wiring substrate is made of resin.

Claim 9 (Canceled).

Claim 10 (Currently Amended): An electronic parts packaging structure according to claim [[1]] 11, wherein the bump of the electronic parts is made of gold, and at least a surface layer portion of the connection pad of the wiring substrate is made of gold.

Claim 11 has been added as follows:

Claim 11 (New): An electronic parts packaging structure comprising:
a wiring substrate which has a structure in which a wiring pattern including a plurality of connection pads on an insulating film, and in which a plurality of via posts are filled in via holes are arranged in portions in the insulating film under the connection pads or under the wiring pattern connected to connection pads within 200 μ m from the connection pads, the via post functioning as

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strut to support the connection pads upon a ultrasonic flip-chip packaging; and
the electronic parts whose bumps are ultrasonic flip-chip packaged to the connection pads;
wherein, the via holes are arranged in a state that dummy via holes and normal via holes are
arranged mixedly, and a normal via holes is arranged separately under the wiring pattern electrically
connected to the dummy via hole, in the wiring pattern in which the via post in dummy via holes is
used as the struts.